Docket No.: 20046/0200688-US0

ABSTRACT

A selection transistor for a group of memory cells, preferably composed of 16-32 memory cells, is respectively introduced into the feed lines to the memory cells. The selection transistor is opened to a line group for reading, while the control gates of all lines are low potential, and the current for each reading column leading through said line group is measured and stored. In a second step, the control gate of the line to be read is brought to a higher reading potential and the resulting current is compared to the previous current.